Solid-state Imaging Device and Control Method for Same

BACKGROUND OF THE INVENTION

1. Technical Field of the Invention

The present invention relates to a solid-state imaging device, such as a CMOS image sensor, having an electronic shutter function, and to a control method for same.

2. Description of the Related Art

Conventionally, the CMOS image sensors mostly have electronic shutter functions. Differently from the CCD image sensors, because of the use of a focal plane shutter (rolling shutter) to reset the signals on a pixel-row basis by sequentially scanning a multiplicity of pixels arranged two-dimensional, there is a problem that exposure time deviates between the rows on the screen.

In this case, when shooting a vertically straight object moving in a horizontal direction, it comes out as if it were inclined.

Fig. 7A is an explanatory figure illustrating such a situation. After resetting the rows, the operation for transfer output (signal reading) is sequentially made on each row after a predetermined exposure time. As a consequence, the image obtained has a vertically straight object a moving sideways taken in an inclined state, as shown in Fig. 7C for example.

On the contrary, there exist those allowing shuttering on all the rows at the same time. In such a case, photodiodes (PDs) are reset simultaneously over all the rows at a certain point of time. After a predetermined exposure time, the charges on the PDs are transferred, simultaneously at all the rows, to a floating diffusion (FD). The FD signals are outputted row by row in the order.

Fig. 7B is an explanatory figure illustrating a situation like that. After resetting all the rows in batch, simultaneous transfer is done on all the rows, followed by an output on a row-by-row basis. By doing so, even in the case of shooting a vertical straight object a moving horizontally, it can be taken straight as it is as shown in Fig. 7D.

Meanwhile, there is a proposal having a transistor (drain Tr) capable of excluding PD extra charge directly onto the drain without passing through the FD, as a pixel circuit configuration for simultaneously resetting, with signal charge, the photodiodes (PDs) of all the pixels on a CMOS image sensor (see Patent Document 1).

[Patent Document 1]

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However, the CMOS image sensor in the all-the-pixel shutter scheme shown in Fig. 7B involves the following problems.

(1) In the duration of after a simultaneous transfer over all the rows and before a sequential output on a pixel-row basis,

light might leak to the FD the amount of which is different between the rows to be outputted earlier and to be outputted later. This results in a worsened photographic image.

(2) Because the PDs are reset after outputting the information of all the rows, exposure is impossible in a duration from a simultaneous transfer over all the rows to a completion of outputting row by row the information of all the rows. This spends time uselessly. Meanwhile, because of difficulty in taking an exposure time period great, the sensitivity lowers where the subject is dark.

These problems are explained below in greater detail.

At first, as for the above (1), there is a difference of one frame-reading time between the row to be outputted at the head and the row to be outputted at the last, in respect of the time length from a transfer to an output. The amount of a leak light to the FD is nearly zero on the head row whereas the amount of a leak light on the last row amounts to one frame-reading time period.

Photoelectric conversion is effected also at the FD, to build up charges at the FD in an amount corresponding to that light amount. This charge is added to the signal charge transferred from the PD.

This results in, besides noise or shading, exceeding the amount of saturation signal to cause white skipping in the case of intense light. In this manner, the leak of light to the FD

considerably worsens the photographic image.

In this relation, explanation is made with using Figs. 8 and 9. Fig. 8 is a sectional view showing a structure of a photodiode peripheral part of the prior-art CCD solid-state imaging device.

The CCD solid-state imaging device has a photodiode (PD) 12, a reading channel part 14, a channel stop part 16, a vertical transfer register 18 and the like, formed in an upper layer region of a semiconductor substrate 10. A polysilicon transfer electrode 22 is arranged on an upper surface of the semiconductor substrate 10 through a gate insulation film 20, on which a shade film 26 is further arranged through an insulation film 24.

In the shade film 26, an opening 26A is formed corresponding to a light-receiving surface of the PD 12. Meanwhile, a planarizing film (upper-layered insulation film) 28 is formed on the shade film 26, on which a color filter 30 and micro-lens 32 is fitted.

In the CCD solid-state imaging device thus configured, the photoelectric charge on the PD 12 is read out simultaneously over the entire screen, and transferred to a vertical transfer register 18 through the reading channel part 14.

Thereafter, the photoelectric charge is conveyed row by row to an output amplifier (not shown) by the CCD of the vertical transfer register 18, then being outputted.

As shown in the figure, on the CCD solid-state imaging device, a metal layer of aluminum or the like to serve as a shade film 26 is formed extending down to an immediate vicinity of the PD 12, to prevent light from leaking to the vertical transfer register 18. Nevertheless, a slight part of light leaks to the vertical transfer register 18. This is responsible for the image deterioration in a vertical-line form, called smear.

Fig. 9 is a sectional view showing a construction of a photodiode peripheral part of the prior-art CMOS solid-state imaging device.

This CMOS solid-state imaging device has P-well regions 42, 44 as a device region formed in an upper-layered part of a semiconductor substrate (N-type silicon substrate) 40, to form a PD 46 and various gate elements in the P-well regions 42, 44. Note that, in the illustrated example, the P-well region 42 is formed therein with a PD 46, a transfer gate (MOS transistor) 48 and an FD 50 while the P-well region 44 is with a MOS transistor 52 of the peripheral circuit section.

Meanwhile, in the above of the semiconductor substrate 40, a polysilicon transfer electrode 56 of each gate is formed through a gate insulation film 54. In the upper layer than that, multi-level wiring layers 60, 62, 64 are formed through an interlayer insulation film 58. Of the multi-level wiring layers, the uppermost-layered film 64 is formed as a shade film.

Meanwhile, on the multi-level wiring layers, a color

filter 72 and micro-lens 74 is arranged through a protection film (SiN) 70.

In this manner, in the CMOS solid-state imaging device, pixels are made by the use of a CMOS process similarly to the peripheral circuits, making it impossible to make a shade film (wiring layer 64) extending down to an immediate vicinity of the PD 46. Thus, it is impossible to fabricate a structure allowing light to enter only the PD 46.

Furthermore, because the metal wiring layer exists in plurality of layers, light is to be irregularly reflected upon the layers. For this reason, a great deal of light is to leak to the FD 50 as compared to the case of a CCD solid-state imaging device, as can be understood from Fig. 9.

Thus, the CMOS solid-state imaging device involves a problem that image deterioration is serious upon simultaneous transfer on all the rows.

Next, as for the above (2), resetting the PD is by draining the charge of the PD to the FD. At this time, in case the FD is in a signal holding state, the signal is to be destroyed. Consequently, PD resetting is possible only after all the rows of FD signal have been read out.

For this reason, there exists a CMOS sensor having a transistor (drain Tr) capable of draining PD extra charge directly to the drain without passage through the FD, as disclosed in the foregoing Patent Document 1. However, this

still requires PD resetting via the FD. Unless the PD is reset after reading FD signals on all the rows, image deterioration results.

This is because of the following reason. Namely, because it is impossible to completely match the characteristics, such as threshold, between the transfer Tr for transferring PD charge to the FD and the drain Tr mentioned in the above. In case the PD is reset in the beginning of a storage time period by the drain Tr, the PD is not return to the reset state when transferring charge to the FD in the end of the storage time period by the transfer Tr. The difference might cause problems, such as fixed-pattern noise and afterimage, not to be removed by the later-processing circuit.

Accordingly, in order to obtain a preferred image, PD reset is not allowed before the FD signal has been read out on all the rows. Because no exposure time is available, sensitivity is lowered.

Furthermore, it has been revealed that, in case the PD is reset in a course of FD signal reading by the drain Tr, there encounters a delicate difference between the pixel status before and after resetting the PD thereby causing a problem that a horizontal line is seen in a relevant part of a photographic image.

Meanwhile, it has been also revealed that, in the presence of a drain Tr, there also encounters a problem that a dark current

occurs at an oxide film interface in the beneath thereof which flows into the PD.

Therefore, it is an object of the present invention to provide a solid-state imaging device capable of relieving the restrictions on exposure time period, securing a sufficient exposure time period on swift operation, relatively reducing the noise amount due to light leak, and outputting a suitable image, in the case of realizing an entire-screen simultaneous shutter function by the use of a solid-state imaging device having such a device structure as the foregoing CMOS solid-state imaging device, and a controlling method for the same.

SUMMARY OF THE INVENTION

The present invention, for achieving the foregoing object, is a solid-state imaging device having an imaging region section provided with a plurality of pixels and a processing circuit section for processing an image signal outputted from the imaging region section, the solid-state imaging device comprising: the pixel having a photoelectric converting element for generating a signal charge commensurate with a light-receiving amount, a floating diffusion part for detecting an amount of a signal charge generated by the photoelectric converting element, a transfer transistor for transferring a signal charge generated by the photoelectric converting element to the floating diffusion part, and a drain transistor for

draining a signal charge generated by the photoelectric converting element; the photoelectric converting element being formed by a buried photodiode having a charge separating region formed by a first conductivity type high-concentration impurity layer in an extreme surface of a semiconductor substrate and a charge storing region formed by a second conductivity type impurity layer in a layer beneath the charge separating region; both a channel potential on the drain transistor being turned on and a channel potential on the transfer transistor being turned on being set higher than a potential for depleting the photodiode.

Meanwhile, the present invention is a control method for a solid-state imaging device having an imaging region section provided with a plurality of pixels and a processing circuit section for processing an image signal outputted from the imaging region section, wherein the pixel has a photoelectric converting element for generating a signal charge commensurate with a light-receiving amount, a floating diffusion part for detecting an amount of a signal charge generated by the photoelectric converting element, a transfer transistor for transferring a signal charge generated by the photoelectric converting element to the floating diffusion part, and a drain transistor for draining a signal charge generated by the photoelectric converting element; the photoelectric converting element being formed by a buried photodiode having

a charge separating region formed by a first conductivity type high-concentration impurity layer in an extreme surface of a semiconductor substrate and a charge storing region formed by a second conductivity type impurity layer in a layer beneath the charge separating region; the control method for a solid-state imaging device comprising: setting both a channel potential on the drain transistor being turned on and a channel potential on the transfer transistor being turned on higher than a potential for depleting the photodiode; and enabling to completely transfer the signal charge of the photodiode through both the transfer transistor and the drain transistor, and starting an exposure operation on the photodiode in a course of reading of the signal charge from the floating diffusion part.

Meanwhile, the present invention is a camera apparatus for outputting an image taken by a solid-state imaging device, the camera apparatus comprising: the solid-state imaging device having an imaging region section provided with a plurality of pixels and a processing circuit section for processing an image signal outputted from the imaging region section, the pixel having a photoelectric converting element for generating a signal charge commensurate with a light-receiving amount, a floating diffusion part for detecting an amount of a signal charge generated by the photoelectric converting element, a transfer transistor for transferring a signal charge generated

by the photoelectric converting element to the floating diffusion part, and a drain transistor for draining a signal charge generated by the photoelectric converting element; the photoelectric converting element being formed by a buried photodiode having a charge separating region formed by a first conductivity type high-concentration impurity layer in an extreme surface of a semiconductor substrate and a charge storing region formed by a second conductivity type impurity layer in a layer beneath the charge separating region; both a channel potential on the drain transistor being turned on and a channel potential on the transfer transistor being turned on being set higher than a potential for depleting the photodiode.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing a configuration example of a camera system in an embodiment of the present invention;

Fig. 2 is a block diagram showing a configuration example of a solid-state imaging device and analog circuit of a camera system shown in Fig. 1;

Fig. 3 is a circuit diagram showing a configuration example of a pixel circuit provided on each pixel of the solid-state imaging device shown in Fig. 2;

Fig. 4 is a timing chart showing the operation of the solid-state imaging device shown in Fig. 2;

Fig. 5 is a sectional view showing a construction of a

PD and its peripheral part of the solid-state imaging device shown in Fig. 2;

Fig. 6 is an explanatory figure showing the potential transition during charge reading on the solid-state imaging device shown in Fig. 2;

Fig. 7 is an explanatory figure showing two kind examples of shutter and signal-reading operations and output images in the prior art;

Fig. 8 is a sectional view showing a layered structure of a CCD solid-state imaging device in the prior art; and

Fig. 9 is a sectional view showing a layered structure of a CMOS solid-state imaging device in the prior art.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now, explanation will be made on the embodiments of a solid-state imaging device, a camera apparatus and a control method for the same according to the invention.

The present embodiment is of a device structure that a CMOS solid-state imaging device has a drain gate and a transfer gate provided on the respective sides of a PD thereof. The charge stored on the PD can be completely reset/transferred at both the drain and transfer gates, thereby enabling to start a storage in a course of reading a signal of the FD.

Meanwhile, dark current can be prevented by applying a negative voltage to the drain and transfer gates.

Fig. 1 is a block diagram showing a configuration example of a camera system according to the embodiment of the present invention.

The camera system includes an imaging lens system 101, a solid-state imaging device 102, an analog circuit 103, an A/D converter 104, a camera signal processing circuit 105, a compressing/expanding circuit 106 and a storage medium 107.

At first, the rays of light incident upon the imaging lens system 101 are focused on a two-dimensional pixel array of the solid-state imaging device 102. The solid-state imaging device 102, a device such as a CMOS image sensor, has an all-the-pixel simultaneous shutter function (reset/transfer at FD) and a row sequential reading function from the FD constituting the features of the present embodiment.

The analog circuit 103 carries out a process, such as CDS (correlated double sampling) and AGC (automatic gain control). The image signal processed by the analog circuit 103 is converted from analog data into digital data by the A/D converter 104, then being outputted to the camera signal processing circuit 105.

The camera signal processing circuit 105 carries out a signal process, such as color signal processing for conversion from output data of the solid-state imaging device 102 into a video signal, gain control processing and white-balance processing.

The compressing/expanding circuit 106 makes a compression or expansion on the image data processed by the camera signal processing circuit 105 and transforms the image into a format to be stored to the storage medium 107. The storage medium 107 is a memory stick, for example, which is an example of means for outputting image data. This may be a display panel, a network in various kinds, or the like.

Fig. 2 is a block diagram showing a configuration example of the solid-state imaging device 102 and analog circuit 103 shown in Fig. 1.

As shown in the figure, the solid-state imaging device of this embodiment has a pixel section (imaging region) 210, a constant current section 220, a column signal processing section (column section) 230, a vertical (V) selection drive means 240, a horizontal (H) selection drive means 250, a horizontal signal line 260, an output processing section 270 and a timing generator (TG) 280 and so on, provided on a semiconductor device substrate 200.

The pixel section 210 is arranged with a multiplicity of pixels in a two-dimensional matrix form, wherein a pixel circuit as shown in Fig. 3 is provided for each pixel. The pixel signals from the pixel section 210 are outputted, on a pixel column basis, to a column signal processing section 230 through a vertical signal line (omitted in Fig. 2).

The constant current section 220 is arranged therein with

constant current sources (omitted in Fig. 2) for supplying bias currents to the pixels, on a pixel column basis.

The V-selection drive means 240 selects, row by row, the pixels of the pixel section 210, to drive-control the shutter operation and reading operation of the pixels.

The column signal processing section 230 receives pixel signals, in an amount of one row a time, obtainable through the vertical signal line and carries out a predetermined signal process column by column, to temporarily hold the signal. For example, it is assumed that properly carried out a CDS (removing fixed pattern noise caused by the threshold variations between the pixel transistors) process, an AGC (auto gain control) process and an A/D conversion process.

The H-selection drive means 250 selects, one by one, a signal of the column signal processing section 230 and directs it onto the horizontal signal line 260.

The output processing section 270 makes a predetermined process on the signal from the horizontal signal line 260 and outputs it to the external, e.g. having a gain control circuit and a color processing circuit. Incidentally, A/D conversion may be by the output processing section 270 in place of the column signal processing section 230.

The timing generator 280 supplies various pulse signals and the like required to operate the sections, on the basis of a reference clock.

Fig. 3 is a circuit diagram showing a configuration example of a pixel circuit provided on each pixel of the solid-state imaging device shown in Fig. 2.

The shown configuration is a provision of a photodiode (PD) 219 and five pixel transistors (Trs) 211, 212, 213, 214, 215 of transfer, amplification, selection, reset and drain, on each pixel.

The PD 219 is to store electrons caused due to photoelectric conversion. By turning on the transfer Tr 211, the electron on the PD 219 is transferred to the floating diffusion (FD) 216. Because the FD 216 possesses a parasitic capacitance, photoelectrons are reserved there.

The amplifying Tr 212 has a gate connected to the FD 216, to convert a potential change on the FD 216 into an electric signal. The selecting Tr 213 selects, row by row, the pixels from which signals are to be read. When the selecting Tr 213 is turned on, the amplifying Tr 212 mates with a constant current source 218 connected outside the pixel to the vertical signal line 217, into a source-follower circuit. Thus, the voltage interactive with a voltage on the FD 216 is outputted onto the vertical signal line.

The reset Tr 214 resets the Vdd wiring with a potential of the FD 216.

The drain Tr 215 resets the power Vdd wiring directly with a photoelectron on the PD 219. The power Vdd wiring is common

between all the pixels.

Meanwhile, the wirings 211A, 213A, 214A for the transfer Tr 211, selecting Tr 213 and reset Tr 214 extend sideways (horizontally = in row direction), to simultaneously drive the pixels included on the same row. This can cope also with driving a focal plane shutter.

Meanwhile, although the wiring 215A for the drain Tr 215 extends vertically, it is short-circuited at the upper and lower ends of the pixel section and hence made common between all the pixels.

The PD 219 employs a buried type PD. The buried type PD, if it is a photodiode in a P-well for example, has a p+ type region nearby the interface of a gate oxide film and an n type region formed in the beneath thereof. Because the interface is covered with the p+ region, dark current can be prevented from occurring at the interface.

Meanwhile, the transfer Tr 211 and the PD 219, if suitably designed, makes it possible to transfer all the photoelectrons of the PD 219 to the FD 216. This is the structure broadly used on the CCD-type sensors, e.g. marketed as a product dubbed HAD (Hole Accumulation Diode).

In the CMOS solid-state imaging device thus configured, the present embodiment is characterized in that the gate voltage and threshold of the Tr 211, 215 as well as the dose to the PD 219 are adjusted such that the channel potentials on the

turned-on drain Tr 215 and turned-on transfer Tr 211 are both higher than a potential for depleting the buried-type PD 219.

Due to this, the transfer Tr 211 is allowed to transfer nearly all the photoelectrons of the PD 219 to the FD 216 while the drain Tr 215 is allowed to exclude nearly all the photoelectrons of the PD 219 onto the drain.

Note that, because, in the case of an image for viewing by the human, e.g. a digital camera, the remaining electrons are satisfactorily about 20 or less, then "nearly completely" is meant to include the case to cause such remaining electrons.

Generally, there is a difficulty in providing, on one buried PD, two Trs both with characteristics for nearly complete transfer. Meanwhile, there are already existing those having a transfer Tr enabling nearly complete transfer. For this reason, the present embodiment realizes nearly complete transfer by raising the gate voltage of the drain Tr 215 during on higher than that of the transfer Tr 211.

Particularly, this is preferably given higher than a power voltage of a digital circuit fabricated with the solid-state imaging device on one chip. Consequently, realization is possible by supplying another power from the external of the solid-state imaging device or internally providing a booster circuit.

Meanwhile, the present inventors have proposd that, in the solid-state imaging device of the above configuration, by

applying a negative voltage (referred herein to as a transfer bias voltage) of -1V during off of the transfer gate electrode, dark current (current having a component of electrons to flow to the PD even in the absence of incident light) be suppressed from occurring at the interface beneath the transfer gate part.

This is because, by biasing the transfer gate electrode toward a negative voltage, a P-type channel is formed at the interface of a gate oxide film in the transfer gate part, thereby preventing a dark current from an interfacial level similarly to the buried PD.

Accordingly, the present embodiment applies a negative voltage to the transfer Tr gate electrode and, likewise, a negative voltage also to the drain Tr gate electrode (referred herein to as a drain bias voltage), thereby properly eliminating the both Trs of dark current. Note that a reference 0V is GND while the P-well region is rendered 0V.

It has been confirmed by the actual measurement that, by thus applying a negative voltage to the drain Tr gate electrode, obtained is the effect equivalent to the case of applying a negative voltage to the transfer Tr gate electrode.

Now, the operation is explained of the solid-state imaging device according to the present embodiment.

Fig. 4 is a timing chart showing the operation of the solid-state imaging device of this embodiment.

At first, the FD 216 is reset and the photoelectrons of

the PD 219 is transferred to the FD 216, simultaneously over all the rows. Specifically, for example, a pulse is fed to the reset wirings 214A on all the rows, to reset the FDs 216 of all the pixels. Furthermore, a pulse is fed to the transfer wirings 211A on all the rows, to transfer the photoelectrons of the PDs 219 of all the pixels to the FDs 216.

Then, the signals of the FDs 216 are read out row by row. Herein, because one frame period is fixed at a certain constant time period, e.g. 1/30 second, the time after having read on all the rows is adjusted by a dummy output or the like.

As mentioned before, the prior art could not have taken an exposure time only in the dummy time period after reading on all the rows. On the contrary, this embodiment can set an exposure time period even during still reading row by row. This is explained in detail in the below.

Herein, a non-exposure time period is assumably taken up to the n-th row of one frame while an exposure time period is taken the duration from then on. Explanation is made on the operation up to the (n - 1)-th row, the operation in the n-th row and the operation in the (n + 1)-th row and the subsequent, in the order.

(1) Up to (n - 1)-th row

When the selecting Tr 213 is turned on, a voltage corresponding to a potential of the FD 216 on the relevant row is outputted onto the vertical signal line 217. This signal

is taken to the row signal processing circuit 230 by a sample hold pulse SHD to be supplied to the row signal processing circuit 230. Then, a reset pulse is fed to reset the FD 216 on that row.

Due to this, a voltage corresponding to the potential for resetting the FD 216 is being outputted onto the vertical signal line 217. This is taken again to the row signal processing circuit 230 by a sample hold pulse SHR to be supplied to the row signal processing circuit 230.

Because the difference between those provides a signal, the row signal processing circuit 230 takes a difference and carries out a signal process as mentioned before.

The drain Tr 215 is off during a time period of reading out to the row signal processing circuit 230 and on in the other time period, to exclude the electrons of the PD 219 to the drain. Because the drain Tr 215 has a gate connected to all the pixels as noted before, all the PDs 219 are reset.

(2) On n-th row

The operation of signal reading out is similar to the foregoing. The drain Tr 215 becomes off without exception, at this row as a boundary. From then on, the photoelectrons of the PD 219 are kept accumulated on the PD 219. Thus, an exposure time period comes.

(3) On (n + 1)-th row and the subsequent

The operation of signal reading out is similar to the

foregoing. Meanwhile, the drain Tr 215 is off at all times.

Fig. 5 is a sectional view showing a structure of the PD and its peripheral part of the solid-state imaging device of this embodiment.

The solid-state imaging device has various elements formed in a P-well region 310 provided in a silicon substrate 300. In Fig. 5, there is shown a region formed with a PD 219, an FD 216, a transfer Tr 211, a reset Tr 214 and a drain Tr 215.

The PD 219 is made as a buried-type (HAD-structured) PD having a p+ region 219A formed in the extreme surface of the silicon substrate 300 and an n region 219B formed in the underneath layer thereof.

The FD 216 is made by an n+ region formed laterally of the PD 219 through the transfer gate part (transfer Tr 211).

The transfer Tr 211 has a transfer gate part made in an intermediate region between the PD 219 and the FD 216, and a transfer electrode 211B formed by a polysilicon film on the upper surface of the silicon substrate 300 through a gate insulation film 320.

The reset Tr 214 has a reset gate part made in a region on the a side opposite to the transfer Tr 211 of the FD 216, and a reset electrode 214B formed by a polysilicon film on the upper surface of the silicon substrate 300 through the gate insulation film 320. The signal charge on the FD 216 is excluded to the drain 214C. This drain 214C is connected to a wiring

for the power source Vdd through a not-shown contact or the like.

The drain Tr 215 has a drain gate made in a region on a side opposite to the transfer Tr 211 of the PD 219, and a drain electrode 215B formed by a polysilicon film on the upper surface of the silicon substrate 300 through the gate insulation film 320. The signal charge on the PD 219 is outputted to the drain 215C. This drain 215C is connected to the wiring for the power source Vdd through a not-shown contact or the like.

Incidentally, although the upper-level layers are provided over the electrodes 211B, 214B, 215B through an insulation film 330, these have no direct bearing on the present invention and hence omitted of explanation.

Fig. 6 is an explanatory figure illustrating the potential transition upon charge reading out on the solid-state imaging device thus structured, showing a potential given positive in a downward direction.

Fig. 6(1) illustrates a potential immediately after resetting all the pixels, wherein photoelectric charge is gradually accumulated on each PD 219. In Fig. 6(2), the transfer Tr 211 is turned on to render a transfer-gate channel voltage as Va, to thereby move the photoelectric charge of the PD 219 to the FD 216.

Fig. 6(3) illustrates a state in a post-transfer non-exposure time, wherein the drain Tr 215 remains off to gradually store photoelectric charge to each PD 219.

Next, Fig. 6(4) illustrates a state the drain Tr 215 is turned on to provide the drain gate with a channel voltage of Vb, thereby outputting the photoelectric charge of the PD 219 to a drain 215C of the drain transistor 215. Note that the transfer Tr 211 and the drain Tr 215 cannot be perfectly matched in their characteristics, thus having different values of Vb and Va (Vb > Va in the illustrated example (downward in Fig. 6)).

The first feature of the present embodiment thus configured lies in that the PD 219 is of an HAD structure and wherein the channel voltage during on of the drain Tr 215 is higher than a potential for depleting the PD 219, enabling to drain nearly all the electrons out of the PD 219. Because this renders the remaining electrons on the PD 219 nearly zero, no great variations occur in the initial state of the PDs 219 even in case there is characteristic variations between the drain Trs 215.

Meanwhile, the second feature lies in that the channel voltage during on of the transfer Tr 211 also is higher than a potential for depleting the PD 219, enabling to transfer nearly all the electrons out of the PD 219. Because this renders the remaining electrons on the PD 219 nearly zero, no great variations occur in the post-transfer state of the PDs 219 even where there is characteristic variations between the transfer Trs 211.

By the two features, the states of the PD 219 at a storage start and after transfer are made nearly the same. Accordingly, despite the both are regulated by the different transistors, preferred image signals are available.

Accordingly, starting an exposure can be regulated by the drain Tr 215 while avoiding image deterioration. As a consequence, exposure can be started even during reading the signals out of the FDs 216 row by row.

Meanwhile, the value of an exposure start row n can be variably controlled depending upon a brightness of a subject. Starting an exposure can be set in any time period within one frame.

Note that, during reading to the column signal processing circuit 230, the drain Tr 215 must be off even in a non-exposure time period. In case it is on in this case, pixel output delicately suffers influence. As a consequence, there arises a slight difference in the output image between the signals of up to the n-th row and of the n-th row and the subsequent, resulting in an appearing horizontal line. In order to prevent this, the drain Tr 215 even in a non-exposure time period is off at least during pixel output, similarly to that in an exposure time period.

In the case of realizing so-called simultaneous shutter that exposure time period at start and end is made simultaneous over the entire screen on a CMOS sensor by the above

configuration and operation, the following effects are obtainable.

(1) Even in case the PD is reset in the course of outputting the information on all the rows, image deterioration can be prevented. Accordingly, in the duration from a simultaneous transfer on all the rows to a completion of outputting row by row, the information on all the rows, utilization is possible for an exposure time period while avoiding image deterioration, enabling to raise sensibility owing to a sufficient exposure time period.

(2) During the operation of the above (1), the photographic image can be prevented from interfered by a horizontal line.

(3) Dark current can be greatly reduced by rendering negative a gate voltage of the drain Tr being off, in addition to the transfer Tr.

Incidentally, the above explanation was concerned on the configuration and operation of the CMOS solid-state imaging device provided on the camera apparatus. However, the present invention can be implemented as a single-bodied solid-state imaging device and a control method for same.

Meanwhile, it is possible to selectively use the foregoing all-the-pixel simultaneous shutter operation and the conventional focal-plane shutter operation. Operation keys or the like can be provided as selecting means, for enabling user's

selection.

Furthermore, concerning an exposure time period as in the above, operation keys or the like can be provided as selecting means, for enabling user's suitable selection. Depending upon an exposure time period selected by the user, it is possible to carry out control in a manner of selecting a start row of exposure as mentioned above.

As explained above, in the solid-state imaging device of the invention and control method for same, there is provided a drain transistor for discharging the signal charge of a buried-type photodiode separately from a transfer transistor for transferring to a floating diffusion part the signal charge of a buried-type photodiode as a photoelectric conversion element on each pixel. By setting both the channel potential on the turned-on drain transistor and the channel potential on the turned-on transfer transistor higher than a potential for depleting the photodiode, the signal charge of the photodiode can be completely transferred from both the transfer transistor and the drain transistor.

Accordingly, in the operation of sequentially reading signal charges on a pixel-row unit basis from the floating diffusion part after carrying out an all-the-pixel simultaneous shutter operation and transfer operation in order for shooting a moving subject without inclination, photodiode exposure operation can be started in a course of the reading operation.

This can secure a sufficient exposure time with swift operation, thereby realizing sensitive, preferred image output. Meanwhile, securing a sufficient exposure time can relatively reduce the amount of a noise due to light leak. In also this respect, preferred image output can be realized.

Meanwhile, in a camera apparatus mounting such a solid-state imaging device, sensitive preferred image output can be similarly realized while securing a sufficient exposure time.

Incidentally, the foregoing "complete depletion" and "complete transfer" do not require a completeness in a literal sense, wherein the term "complete" was used as an ideal state. The remaining charge is allowed to exist within a range not to pose a problem of noise.

In addition, the solid-state imaging device is not limited to a device in the form of one chip but may be a chip for signal processing or a camera module device having a desired optical system.